Opportunità di stage

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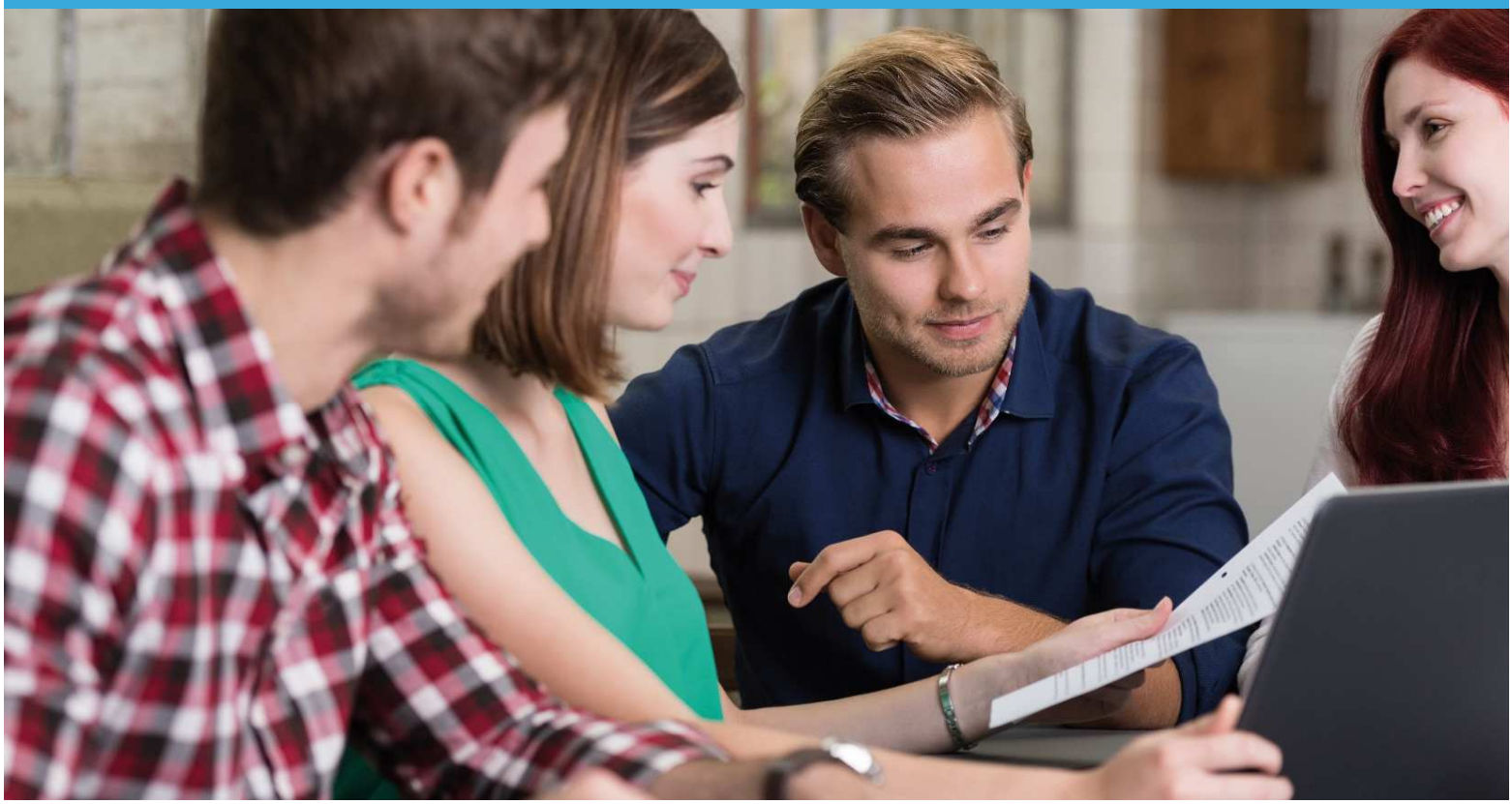

SystemVerilog Structural Netlist approach for Real Number Modeling

Semiconductor industry grow a lot in the last years. All the modern IPs contain several circuitry including Analog and Digital parts. Thus, the need of a verification methodology for the validation and the integration of analog circuits within the digital simulation environment involved more interest and efforts. Mixed signal IPs design and verification have become increasingly complex and compute intensive. The process of the verification can be really challenging due to this aspects. The SystemVerilog Real Number Modeling (RNM) approach uses real variables to model complex Mixed-Signal IPs in order to decrease simulation rate during Analog Mixed-Signal (AMS) simulation and to create a fully digital environment for the Digital Mixed-Signal (DMS) simulations.

Cosa potrai fare?

In this context, we are looking for a thesis student willing to **explore new techniques to develop Analog SystemVerilog Models from existing schematic netlist.** The candidate will be involved in all the steps of model design, from the analog spec to the definition of the capabilities of the model using state-of-the-art CAD suites. The scope of this thesis is developing a method to extract a SystemVerilog model from spice netlist and evaluate the advantages and dis-vantages of using this approach respect to the classic modeling flow.

Cosa ti chiediamo?

If you are a student of Engineering Faculty with:

- Basic knowledge of Analog and Digital design
- a hand-on experience with HDL (Verilog, VHDL)
- Basic Knowledge of Virtuoso simulation environment

Manda il tuo Curriculum a: giuseppe-hr.finocchiaro@st.com
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