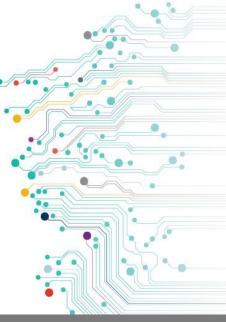


UNIVERSITÀ DEGLI STUDI DI PALERMO



## UNIPA – VIALE DELLE SCIENZE (EDIF. 9, EX DEIM) <u>Rad-hard semiconductor components</u> <u>for space applications</u>

Martedì 3 marzo 2020 alle ore 11.30 presso l'Aula Savagnone del Dipartimento di Ingegneria (Edif. 9, ex DEIM),

## l'Ing. Cristiano Calligaro

**Chief Executive Officer** di **RedCat Devices Srl**, Milano, Italy, terrà un Seminario relativo alla progettazione di componenti elettronici per applicazioni spaziali resistenti alle radiazioni.

La durata del Seminario è di circa 2 ore. Potrà essere accreditato 1 c.f.u. agli studenti partecipanti (dietro presentazione di una breve relazione).

La partecipazione al Seminario è consigliata agli studenti del **terzo anno** della **Laurea Triennale** e agli studenti della **Laurea Magistrale** in **Ingegneria Elettronica**. La partecipazione di studenti e docenti di altri corsi di Laurea è benvenuta.



Per info rivolgersi a: <u>Prof. Giuseppe Lullo</u> <u>Prof. Costantino Giaconia</u>

## Argomenti trattati:

Semiconductor components to be used in space applications have as a major constraint the need to be resilient against radiations. Total lonizing Dose (TID) and Single Event Effects (SEE) come from energetic particles interacting with silicon devices and produce both hard errors (Latch-up, degradation of oxides) and soft errors (bit flip of memory elements and transient propagation). To mitigate such effects very tailored design techniques are adopted (Radiation Hardening by Design or simply RHBD) making leverage on standard and well consolidated silicon process (mainly CMOS).

In this tutorial the major effects on the interaction between charged particles and silicon devices will be presented together with the most common techniques to make a mitigation according to the expected mission (low orbits, high orbits, deep space). Design techniques at circuit level (smart schematics) and at layout level (robust layouts) will be mentioned with a specific focus on digital building blocks (standard cells, embedded SRAMs) used for larger mixed signal ASICs (microcontrollers, core processors, imagers, DSPs). In the last part of the tutorial some "real world" examples will be shown together with a list of the major Free Open Source (FOS) CAD tools available.

**Speaker's short bio**: Cristiano Calligaro received the laurea degree in Electronic Engineering and the Ph.D. degree in Electronics and Information Engineering from the University of Pavia (Italy) in 1992 and 1997 respectively. After obtaining the Ph.D. degree he moved to MAPP Technology. In 2006 he established RedCat Devices srl as a start-up. During his career he has been involved in memory design (volatile and non-volatile) both for consumer application (multilevel flash memories) and space applications (rad-hard memories) and software design for SEE evaluation using free CAD tools (Open Circuit Design). His current research interest is focused on rad-hard libraries for mixed signal ASICs, stand-alone memories (SRAMs and NVMs) and testing methodologies for rad-hard components. He holds 20 patents mainly in the field of multilevel NVMs and is co-author of more than 50 papers and one book (Rad-hard Semiconductor Memories, River Publishers). He has been coordinator of RAMSES and ATENA projects inside the Italy-Israel Cooperation Programme, SkyFlash project in the European FP7 Programme and EuroSRAM4Space project in the European FP7 Programme and EuroSRAM4Space project in the European.